# Si3402B-EVB

## NON-ISOLATED EVALUATION BOARD FOR THE Si3402B

## 1. Description

The Si3402B non-isolated evaluation board (Si3402B-EVB Rev 2) is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application. The Si3402B is described more completely in the data sheet and application notes. This document describes the evaluation board. An evaluation board demonstrating the isolated application is described in the Si3402B-ISO-EVB user's guide.

## 2. Si3402B Board Interface

Ethernet data and power are applied to the board through the RJ45 connector (J1). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary is brought out to the test points. Power may be applied in the following ways:

- Connecting a dc source to pins 1, 2 and 3, 6 of the Ethernet cable (either polarity)
- Connecting a dc source to pins 4, 5 and 7, 8 of the Ethernet cable (either polarity)
- Using an IEEE 802.3-2015-compliant, PoE-capable PSE, such as Trendnet TPE-1020WS

The Si3402B-EVB board schematics and layout are shown in Figures 1 through 6. The dc output is at connectors J11(+) and J12(–).

Boards are generally shipped configured to produce +5 V output voltage but can be configured for +3.3 V or other output voltages by changing resistors R5 and R6. Refer to "AN956: Using the Si3402B PoE PD Controller in Isolated and Non-Isolated Designs" for more information. The preconfigured Class 3 signature can also be modified according to Table 3 in AN956. The D8–D15 Schottky type diode bridge bypass is recommended only for higher power levels (Class 3 operation). For lower power levels, such as Class 1 and Class 2, the diodes can be removed. When the Si3402B is used in external diode bridge configuration, it requires that at least one pair of the CTx and SPx pins be connected to the PoE voltage input terminals (to the input of the external bridge).


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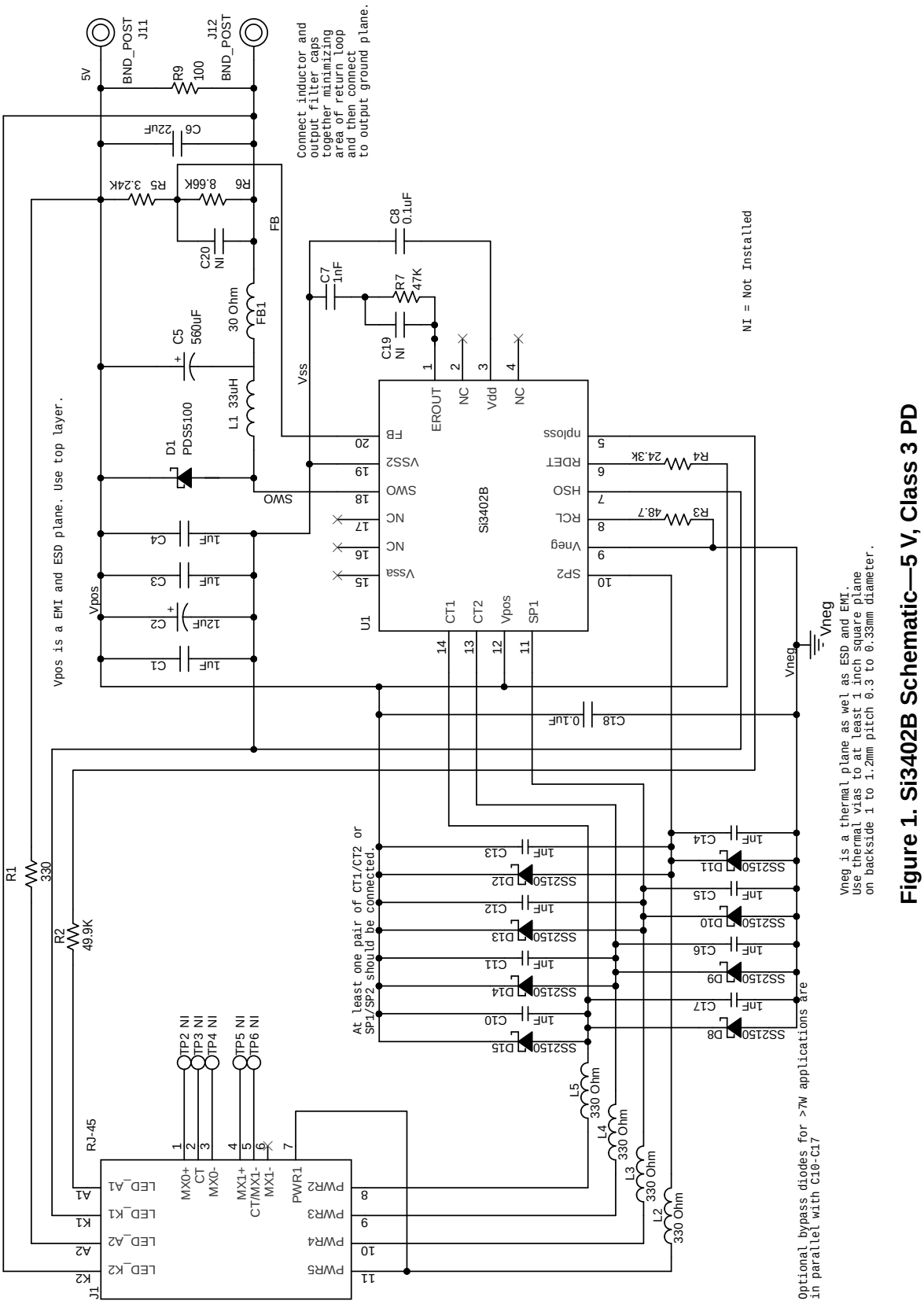



**Figure 1. Si3402B Schematic—5 V, Class 3 PD**

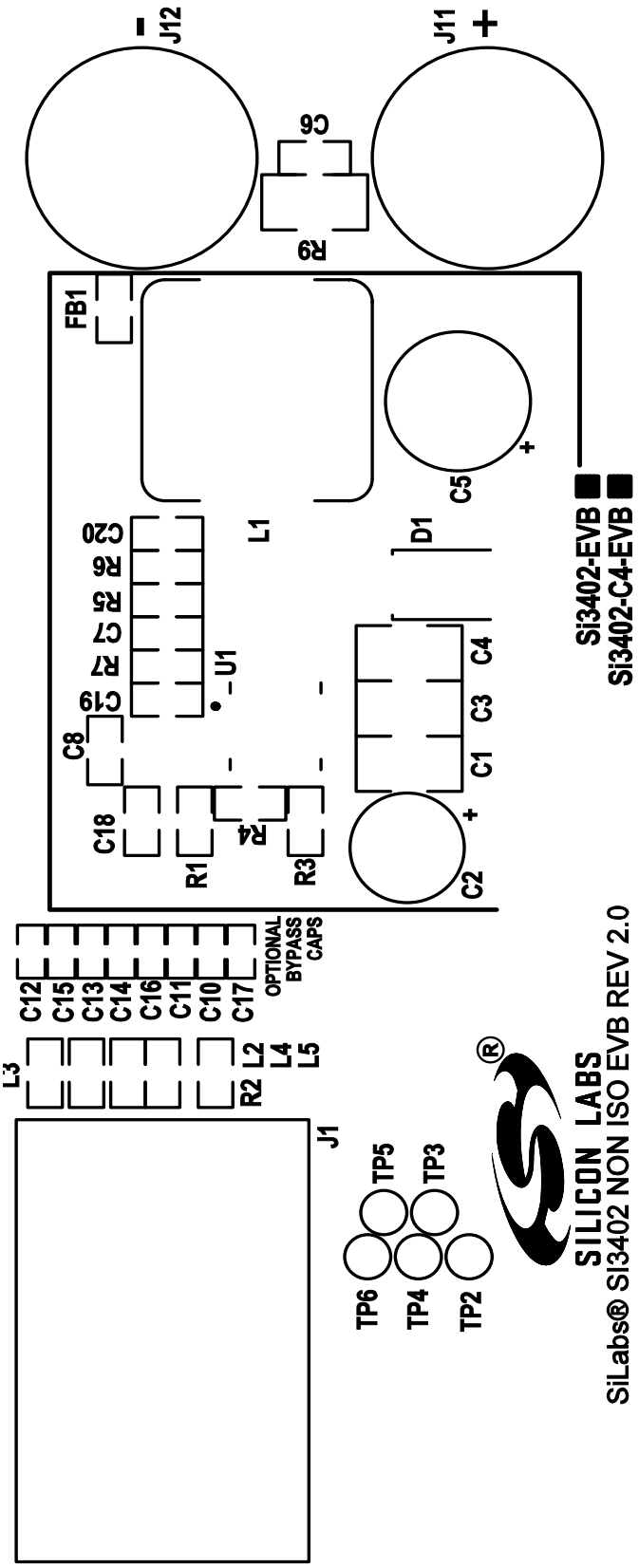



Figure 2. Top Silkscreen

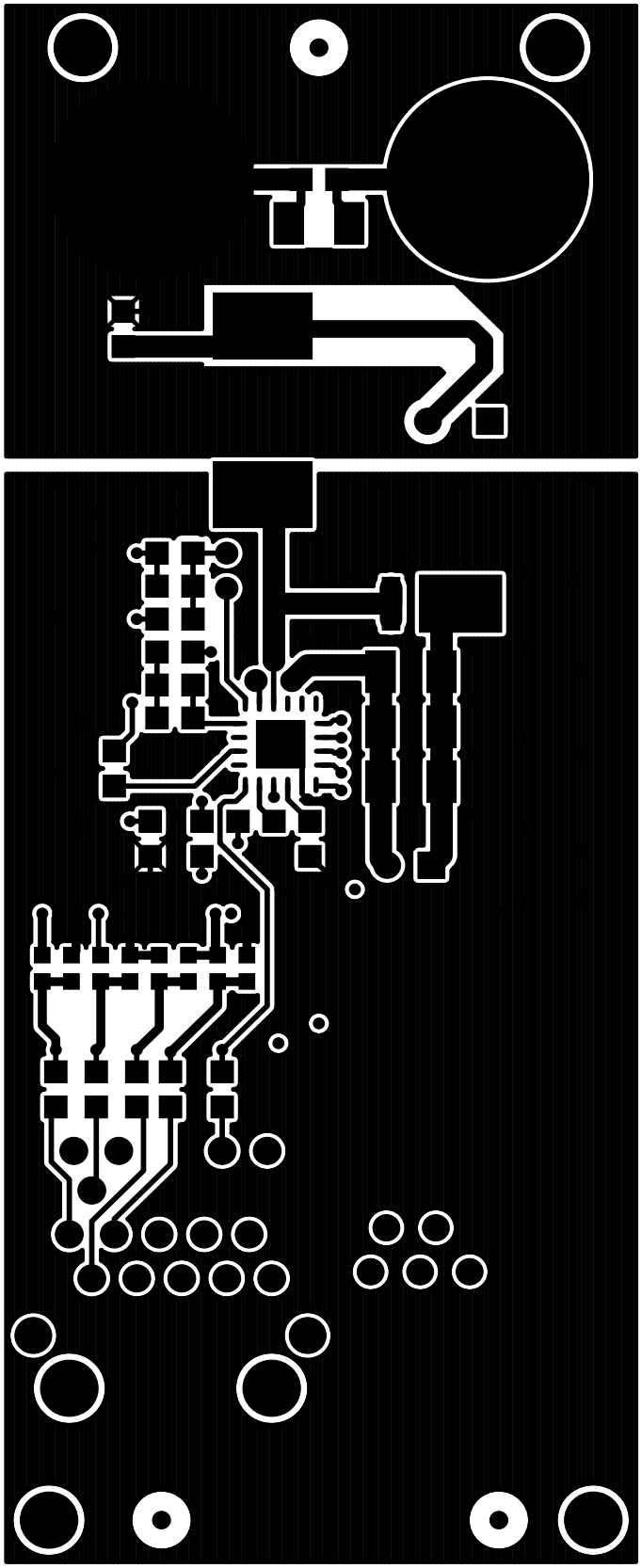


Figure 3. Top Layer

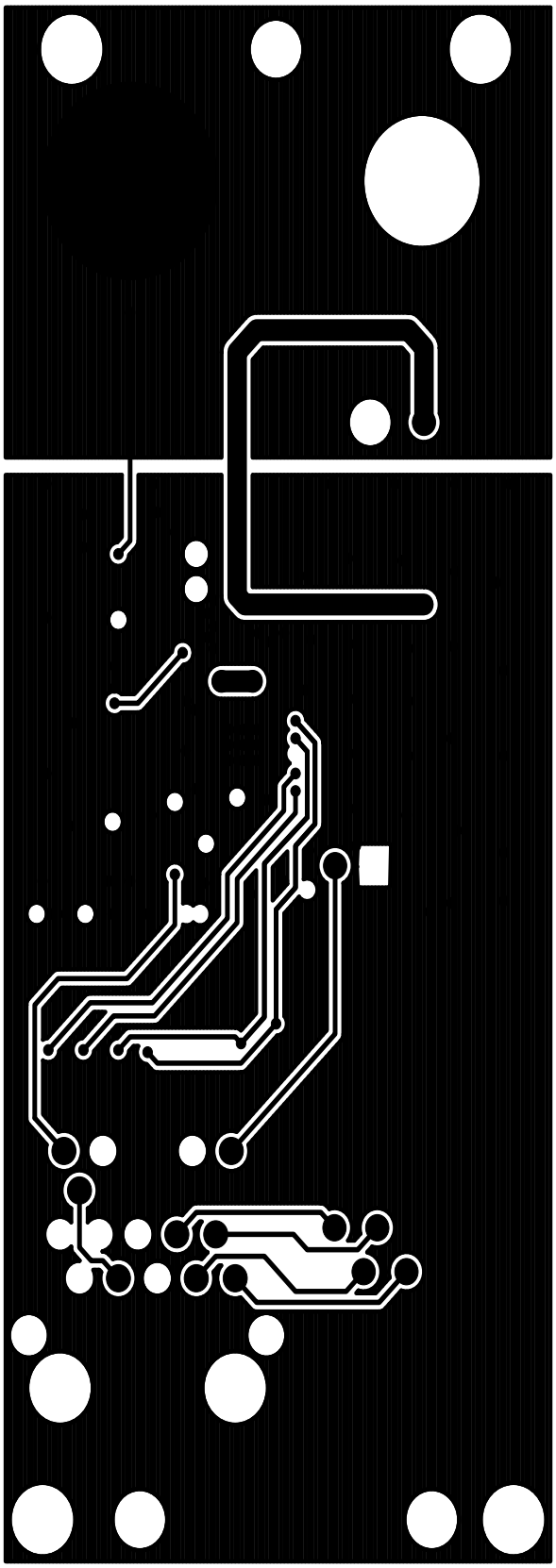


Figure 4. Internal 1 (Layer 2)

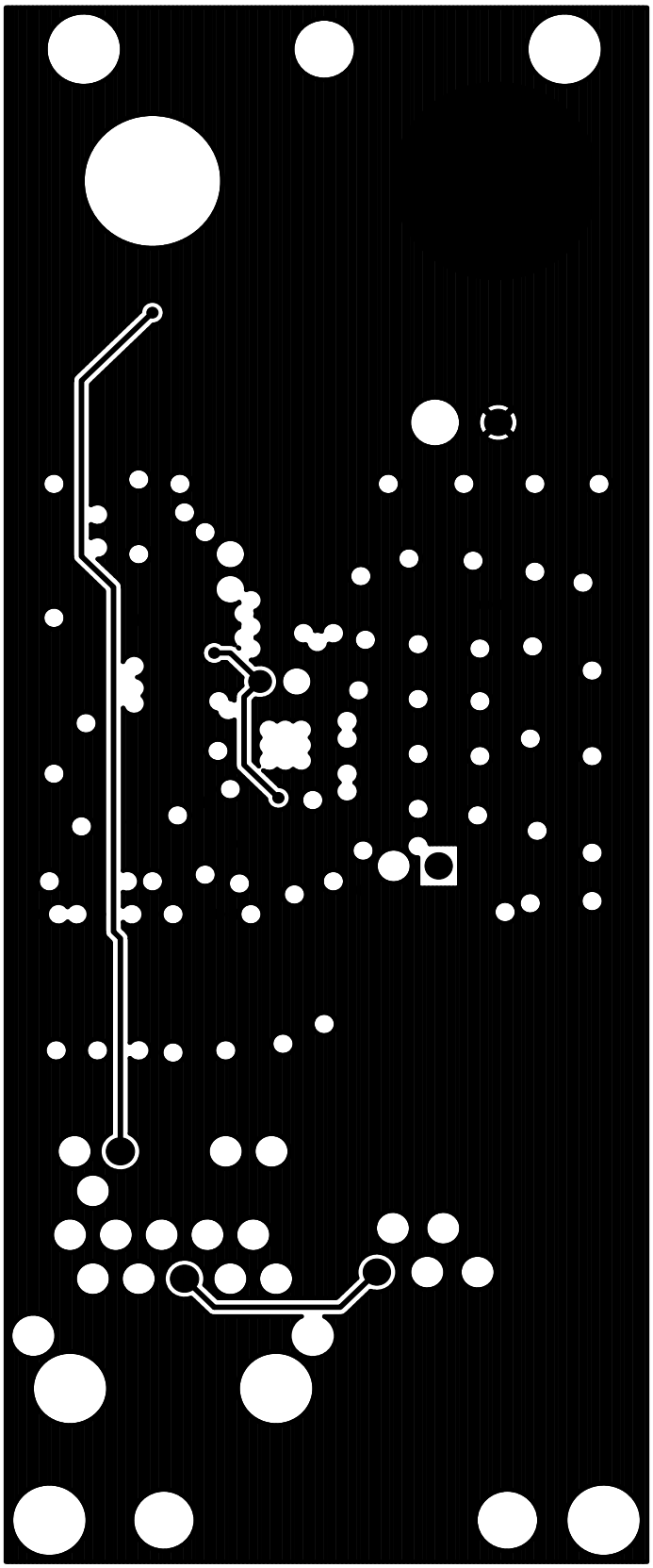


Figure 5. Internal 2 (Layer 3)

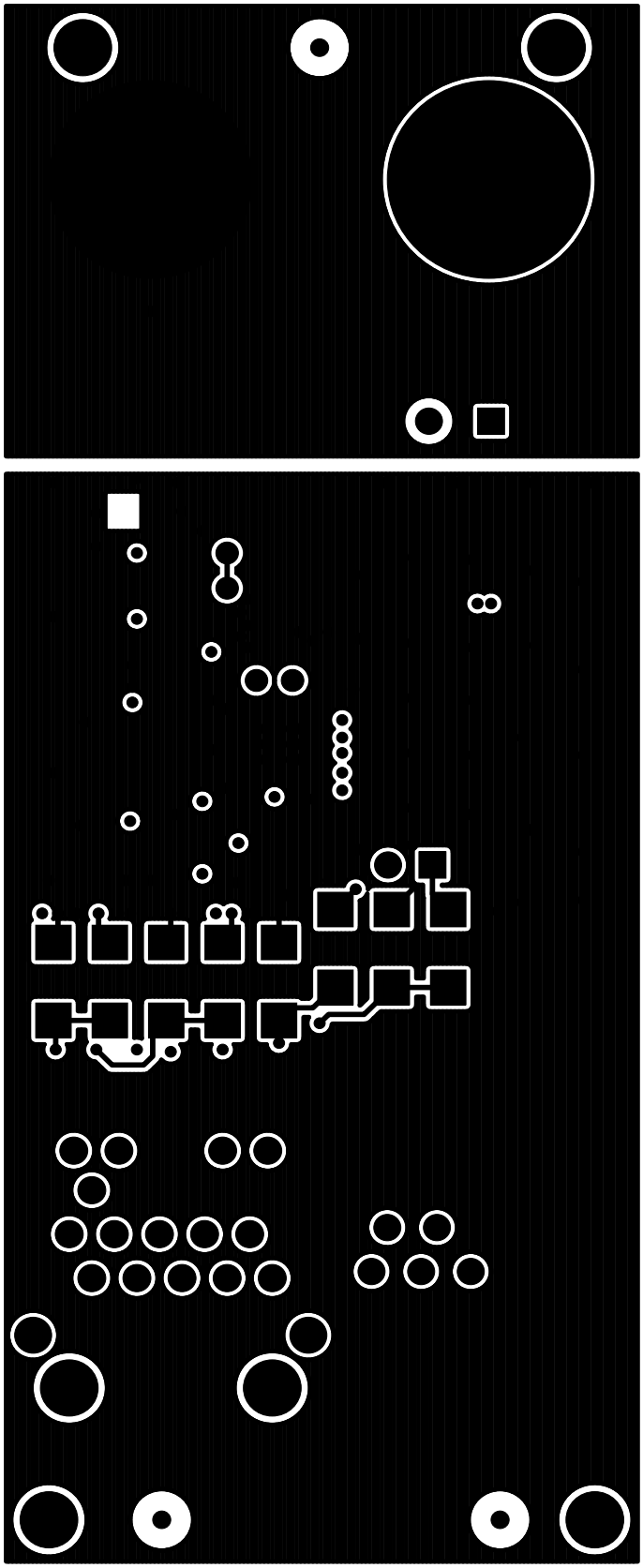


Figure 6. Bottom Layer

## 3. Bill of Materials

The table below is the BOM listing for the standard 5 V evaluation board with a popular option for Class 3. For Class 1 and Class 2 designs, in addition to updating the classification resistor (R3), the external diode bridge (D8–D15) can be removed to reduce BOM costs.

**Table 1. Si3402B-EVB Bill of Materials**

| NI | Qty | Value | Ref | Rating | V | Tol | Type | PCB Footprint | Mfr Part Number | Mfr |
|---|---|---|---|---|---|---|---|---|---|---|
| | 3 | 1 µF | C1, C3, C4 | | 100 V | ±10% | X7R | C1210 | C1210X7R101-105K | Venkel |
| | 1 | 12 µF | C2 | | 100 V | ±20% | Alum_Elec | C2.5X6.3MM-RAD | EEUFC2A120 | Panasonic |
| | 1 | 560 µF | C5 | | 6.3 V | ±20% | Alum_Elec | C3.5X8MM-RAD | EEUFM0J561 | Panasonic |
| | 1 | 22 µF | C6 | | 6.3 V | ±20% | X5R | C0805 | C0805X5R6R3-226M | Venkel |
| | 1 | 1 nF | C7 | | 50 V | ±1% | C0G | C0805 | C0805C0G500-102F | Venkel |
| | 1 | 0.1 µF | C8 | | 16 V | ±10% | X7R | C0805 | C0805X7R160-104K | Venkel |
| | 8* | 1 nF | C10, C11, C12, C13, C14, C15, C16, C17 | | 100 V | ±10% | X7R | C0603 | C0603X7R101-102K | Venkel |
| | 1 | 0.1 µF | C18 | | 100 V | ±10% | X7R | C0805 | C0805X7R101-104K | Venkel |
| NI | 1 | 150 pF | C19 | | 16 V | ±10% | X7R | C0805 | C0805X7R160-151K | Venkel |
| NI | 1 | 3.3 nF | C20 | | 16 V | ±10% | X7R | C0805 | C0805X7R160-332K | Venkel |
| | 1 | PDS5100 | D1 | 5 A | 100 V | | Schottky | POWERDI-5 | PDS5100H-13 | Diodes Inc. |
| | 8 | SS2150 | D8, D9, D10, D11, D12, D13, D14, D15 | 2 A | 150 V | | Single | DO-214AC | SS2150-LTP | MCC |
| | 1 | 30 Ω | FB1 | 3000 mA | | | SMT | L0805 | BLM21PG300SN1 | Murata |
| | 1 | RJ-45 | J1 | | | | Receptacle | RJ45-SI-52004 | SI-52003-F | Bel |
| | 2 | BND_POST | J11, J12 | 15 A | | | Banana | Banana Jack | 101 | Abbatron Hh Smith |
| | 1 | 33 µH | L1 | 5.2 A | | ±20% | Shielded | IND-SPD | MSS1278-333ML | Coilcraft |
| | 4 | 330 Ω | L2, L3, L4, L5 | 1500 mA | | | SMT | L0805 | BLM21PG331SN1 | MuRata |
| | 1 | 330 Ω | R1 | 1/10 W | | ±1% | ThickFilm | R0805 | CR0805-10W-3300F | Venkel |
| | 1 | 49.9 kΩ | R2 | 1/8 W | | ±1% | ThickFilm | R0805 | CR0805-8W-4992F | Venkel |
| | 1 | 48.7 Ω | R3 | 1/8 W | | ±1% | ThickFilm | R0805 | CRCW080548R7FKTA | Vishay |
| | 1 | 24.3 kΩ | R4 | 1/8 W | | ±1% | ThickFilm | R0805 | CRCW080524K3FKEA | Vishay |
| | 1 | 3.24 kΩ | R5 | 1/8 W | | ±1% | ThickFilm | R0805 | CRCW08053K24FKEA | Vishay |
| | 1 | 8.66 kΩ | R6 | 1/10 W | | ±1% | ThickFilm | R0805 | CR080510W-8661F | Venkel |
| | 1 | 47 kΩ | R7 | 1/10 W | | ±5% | ThickFilm | R0805 | CR0805-10W-473J | Venkel |
| | 1 | 100 Ω | R9 | 1/2 W | | ±1% | ThickFilm | R1210 | CR1210-2W-1000F | Venkel |
| NI | 5 | Black | TP2, TP3, TP4, TP5, TP6 | | | | Loop | Testpoint | 5001 | Keystone |
| | 1 | Si3402B | U1 | | 100 V | | PD | QFN20N5X5P0.8 | Si3402B | SiLabs |

***Note:** C10–C17 are populated by default. See the “Surge” section in AN956 for more information.

## 4. BOM Options

The Si3402B non-isolated EVB has been compensated for eight different output voltage and filter combinations:

- 3.3 V output standard ESR 1000 µF 6.3 V filter
- 5 V output standard ESR 1000 µF 6.3 V filter
- 9  output standard ESR 470 µF 16 V filter
- 12 V output standard ESR 470 µF 16 V filter
- 3.3 V output low ESR 560 µF 6.3 V filter
- 5 V output low ESR 560 µF 6.3 V filter
- 9 V output low ESR 330 µF 16 V filter
- 12 V output low ESR 330 µF 16 V filter

For the standard ESR capacitor, the ESR increase at very low temperatures may cause a loop stability issue. A typical evaluation board has been shown to exhibit instability under very heavy loads at –20 °C. Due to self-heating, this condition is not a great concern. However, using a low ESR filter capacitor solves this problem (but requires some recompensation of the feedback loop). The low ESR capacitor also improves load transient response and output ripple.

The Si3402B (non–isolated) EVB was designed with a very simple compensation consisting of R7 and C7.

The standard evaluation board is optimized for a standard ESR filter capacitor for 5 V output.

The following table gives the options that have been tested for other situations.

| $V_{OUT}$ | R6 (To Adjust Output Voltage) | Filter Cap C5 (Type FM are Low ESR) | Filter Cap Part Number (Panasonic) | R7 | C7 |
|---|---|---|---|---|---|
| 3.3 V | 4.64 kΩ | 1000 µF, 6.3 V | ECA0JM102 | 47 kΩ | 1 nF |
| 3.3 V | 4.64 kΩ | 560 µF, 6.3 V | EEUFM0J561 | 47 kΩ | 1 nF |
| 5.0 V | 8.66 kΩ | 100 0 µF, 6.3 V | ECA0JM102 | 47 kΩ | 1 nF |
| 5.0 V | 8.66 kΩ | 560 µF, 6.3 V | EEUFM0J561 | 47 kΩ | 1 nF |
| 9.0 V | 18.2 kΩ | 470 µF, 16 V | ECA1CM471 | 47 kΩ | 1 nF |
| 9.0 V | 18.2 kΩ | 330 µF, 16 V | EEUFM1C331 | 47 kΩ | 1 nF |
| 12.0 V | 25.5 kΩ | 470 µF, 16 V | ECA1CM471 | 47 kΩ | 1 nF |
| 12.0 V | 25.5 kΩ | 330 µF, 16 V | EEUFM1C331 | 47 kΩ | 1 nF |

# APPENDIX—Si3402B DESIGN AND LAYOUT CHECKLIST

## Introduction

Although the EVB design is pre-configured as a Class 3 PD with 5 V output, the schematics and layouts can easily be adapted to meet a wide variety of common output voltages and power levels.

The complete EVB design databases for the standard 5 V/Class 3 configuration are located at www.silabs.com/PoE under the “Documentation” link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Following are recommended design checklists that can assist in trouble-free development of robust PD designs.

Refer also to the Si3402B data sheet and AN956 when using the following checklists.

1. **Design Planning Checklist:**
    a. Determine if your design requires an isolated or non-isolated topology. For more information, see Section 4 of AN956.
    b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3402B into your system design process.
    c. Determine your load’s power requirements (i.e., $V_{OUT}$ and $I_{OUT}$ consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3402B, choose the highest voltage used in your PD and then post regulate to the lower supply rails, if necessary.
    d. If your PD design consumes $\geq$7 W, be sure to bypass the Si3402B’s on-chip diode bridges with external Schottky diode bridges or discrete diodes. Bypassing the Si3402B’s on-chip diode bridges with external bridges or discrete Schottky diodes is required to help spread the heat generated in designs dissipating $\geq$7 W.
    e. Based on your required PD power level, select the appropriate class resistor value by referring to Table 3 of AN956. This sets the Rclass resistor (R3 in Figure 1 on page 2).
2. General design checklist items:
    a. ESD caps (C10–C17 in Figure 1) are strongly recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.
    b. If your design uses an AUX supply, be sure to include a 3 W surge limiting resistor in series with the AUX supply for hot insertion. Refer to AN956 when AUX supply is 48 V.
    c. Silicon Labs strongly recommends the inclusion of a minimum load (250 mW) to avoid switcher pulsing when no load is present and to avoid false disconnection when less than 10 mA is drawn from the PSE. If your load is not at least 250 mW, add a resistor load to dissipate at least 250 mW.
    d. If using PLOSS function, make sure it’s properly terminated for connection in your PD subsystem. If PLOSS is not needed, leave this pin floating.
3. Layout guidelines:
    a. Make sure VNEG pin of the Si3402B is connected to the backside of the QFN package with an adequate thermal plane, as noted in the data sheet and AN956.
    b. Keep the trace length from connecting to SWO and retuning to Vss2 as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.
    c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.

d. Keep the circular area of the loop from the Switcher FET output to the inductor or transformer and returning from the input filter capacitors (C1–C4) to Vss2 as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor or transformer to the Schottky diode and returning through the first stage output filter capacitor back to the inductor or transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.

e. Keep the high power traces as short as possible.

f. Keep the feedback and loop stability components as far from the transformer/inductor and noisy power traces as possible.

g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

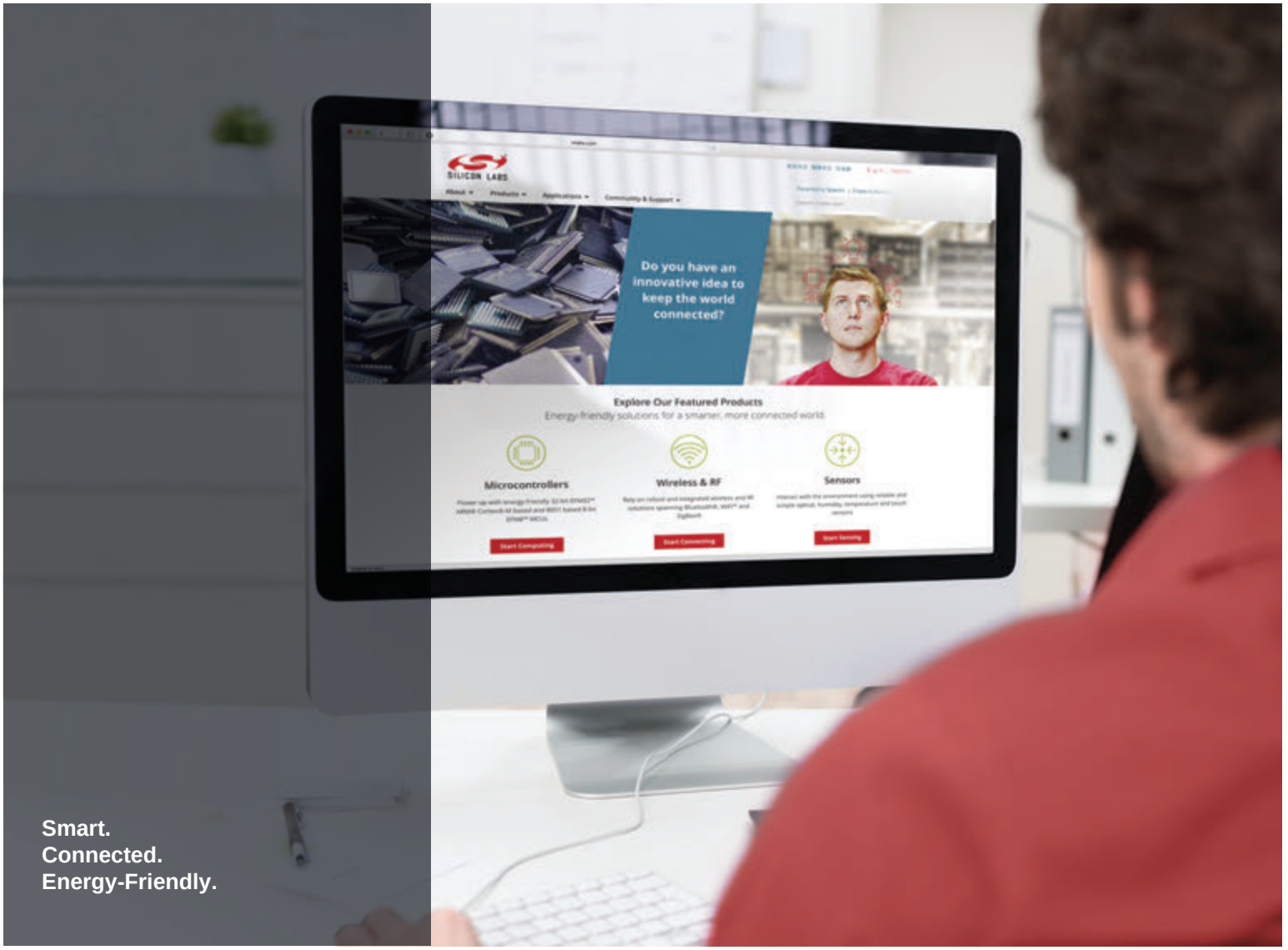
h. As a convenience in layout, please note that the IC is symmetrical with respect to CT1, CT2, SP1, and SP2. These leads can be interchanged. At least one pair of CT1/CT2 or SP1/SP2 should be connected.

To help ensure first-pass success, submit your schematics and layout files to PoEInfo@silabs.com for review. Other technical questions may be sent to this e-mail address as well.

# Document Change List

## Revision 1.0 to Revision 1.1

- Initial release of Si3402B-EVB User's Guide, modified from Si3402-EVB User's Guide Revision 1.0.




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